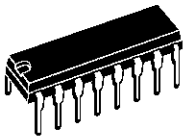
64 STAGE STATIC SHIFT REGISTER

- FULLY STATIC OPERATION 16 MHz (Typ.) at V_{DD} - V_{SS} = 15V
- STANDARD TTL DRIVE CAPABILITY ON Q OUTPUT
- RECIRCULATION CAPABILITY
- THREE CASCADING MODES :
  DIRECT CLOCKING FOR HIGH SPEED OPERATION
  DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS
  ADDITIONAL 1/2 STAGE FOR SLOWS CLOCKS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
  I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

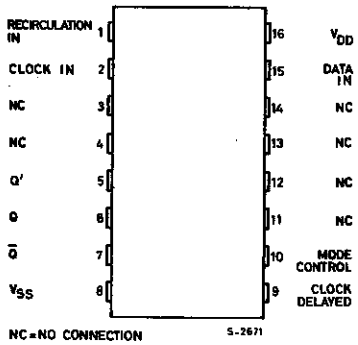
ORDER CODES

PACKAGE	TUBE	T & R
DIP	CC4031	

DESCRIPTION

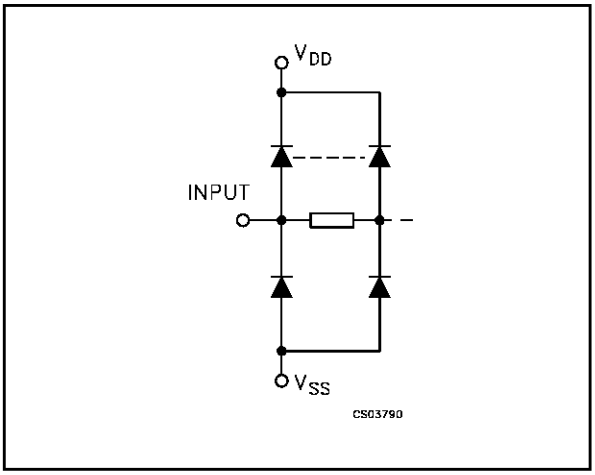
The CC4031 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.
This device is a static shift register that contains 64 D-type, master slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage). The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive going-clock transition. Maximum clock frequencies up to 16 MHz (Typ.) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CC4031 has a MODE CONTROL input that, when in the high state, allows operation in the recirculation mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register

PIN CONNECTION



packages while allowing reduced clock drive fan-out and transition time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative going transition of the clock after the Q output occurs. This delayed output, like the delayed clock (CL_D), is used with clocks having slow rise and fall times.

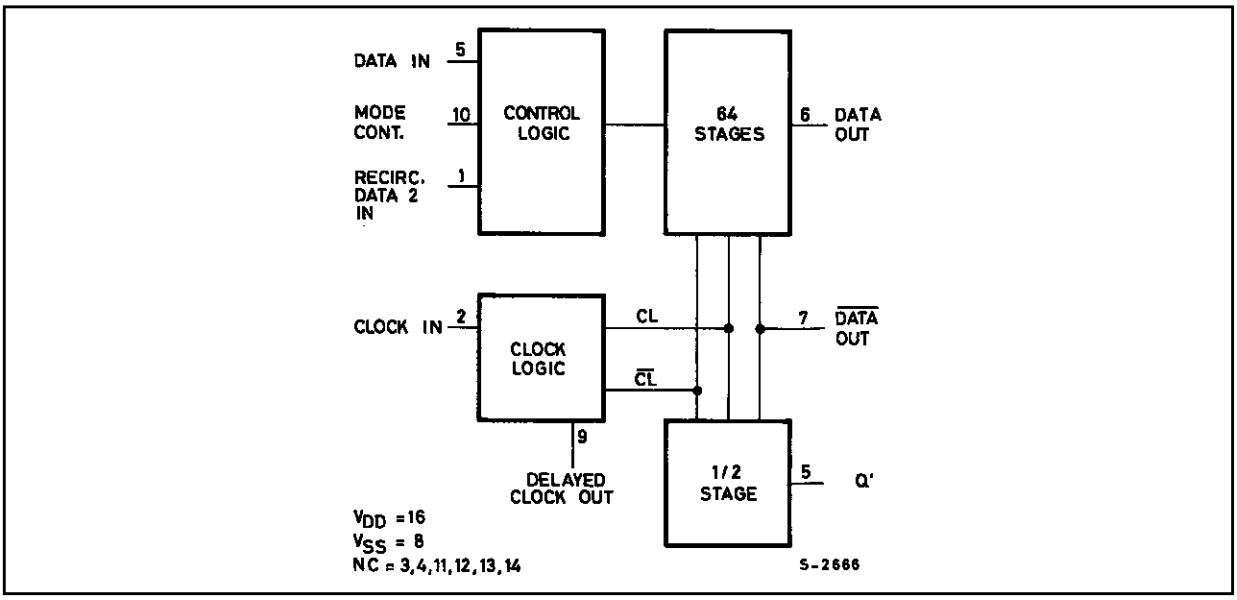
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
15	DATA IN	Data Input
2	CLOCK	Clock Input
10	MODE CON-TROL	Mode Control Input
9	CLOCK DELAYED	Delayed Clock Output
1	RECIRCU-LATIO IN	Recirculation Data In
5, 6, 7	Q', $\overline{Q}$, Q	Data Outputs
3, 4, 11, 12, 13, 14	NC	Not Connected
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



TRUTH TABLES

Input Control Circuit

DATA	RECIRCULATION	MODE CONTROL	BIT INTO STAGE 1
H	X	L	H
L	X	L	L
X	H	H	H
X	L	H	L

Typical Stage

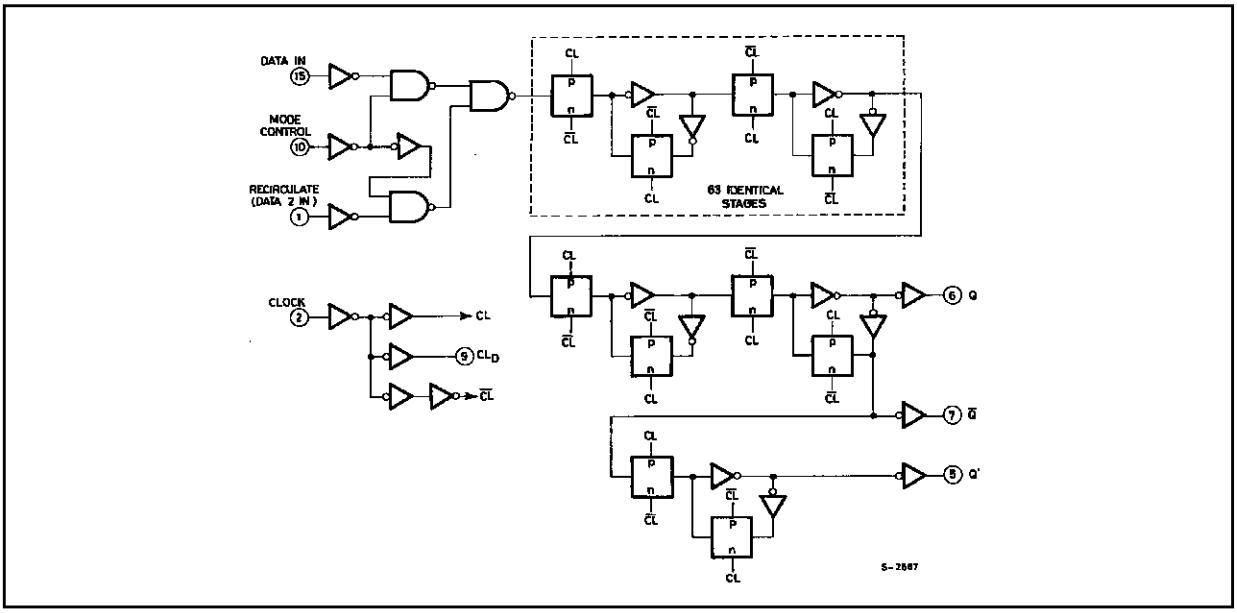
DATA	CLOCK	DATA+1
L	⌐¬	L
H	⌐¬	H
X	¬⌐	NC

Output from Q'

DATA+64	CLOCK	DATA+64.5
L	¬⌐	L
H	¬⌐	H
X	⌐¬	NC

X : Don't Care
NC : No Change

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 1 8	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/18			18		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current (Source) Q, Q, Q' CL_D	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current Q	0/5	0.4	<1	5	1.74	4		1.43		1.43		mA
		0/10	0.5	<1	10	4.42	10.4		3.74		3.74		
		0/15	1.5	<1	15	11.56	27.2		9.52		9.52		
I_{OL}	Output Sink Current Q, Q', CL_D	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL}, t_{PLH}, t_{PLH}	Propagation Delay Time : Clock to Q', Clock to Q	5			250	500	ns
		10			110	220	
		15			90	180	
t_{PHL}, t_{PLH}, t_{PHL}	Propagation Delay Time : Clock to Q', Clock to Q	5			190	380	ns
		10			80	160	
		15			65	130	
	Propagation Delay Time : Clock to CL_D	5			100	200	ns
		10			50	100	
		15			40	80	
t_{THL}', t_{TLH}	Transition Time : (any output, except Q)	5			100	200	ns
		10			50	100	
		15			40	80	
t_{THL}	Transition Time : (Q)	5			50	100	ns
		10			25	50	
		15			20	40	
t_{setup}	Data Setup Time	5			30	60	ns
		10			15	30	
		15			10	20	
t_{hold}	Data Hold Time	5			30	60	ns
		10			15	30	
		15			10	20	
t_W	Clock Pulse Width	5			120	240	ns
		10			50	100	
		15			40	80	
f_{MAX} (2)	Maximum Clock Input Frequency	5		2	4		MHz
		10		5	10		
		15		6	12		
t_r , t_f (1)	Clock Input Rise or Fall Time	5				1000	µs
		10				1000	
		15				200	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) If more than one unit is cascaded, in the parallel clocked application, trCL should be made less than or equal to the sum of the propagation delay at 50pF and the transmission time of the output driving stage.
(2) Maximum Clock Frequency for cascaded units;

a) Using Delayed Clock Feature in Recirculation Mode :

$$f_{MAX} = \frac{1}{(n-1)\ \text{CLD prop. delay} + \text{Q prop. delay} + \text{setup time}}$$ where n = number of packages

b) Not Using Delayed Clock :

$$f_{MAX} = \frac{1}{\text{propagation delay} + \text{setup time}}$$