

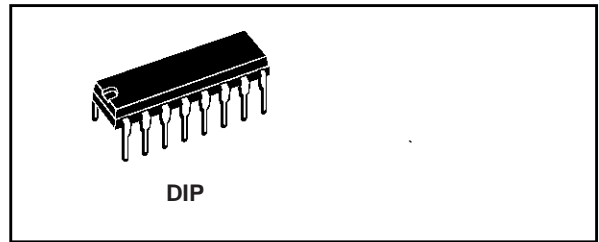


## TRIPLE SERIAL ADDER

- INVERT INPUTS ON ALL ADDERS FOR SUM COMPLEMENTING APPLICATIONS
- FULLY STATIC OPERATION...DC TO 10MHz (Typ.) at  $V_{DD} = 10V$
- BUFFERED INPUTS AND OUTPUTS
- SINGLE PHASE CLOCKING
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT LEAKAGE CURRENT  
 $I_l = 100nA$  (MAX) AT  $V_{DD} = 18V$   $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

The CC4038 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The CC4038 consists of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented.

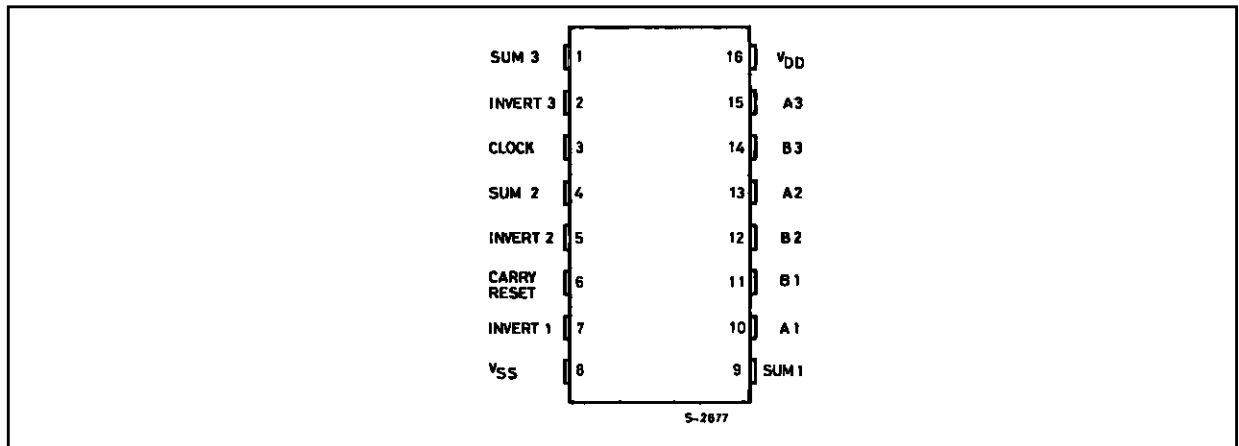


### ORDER CODES

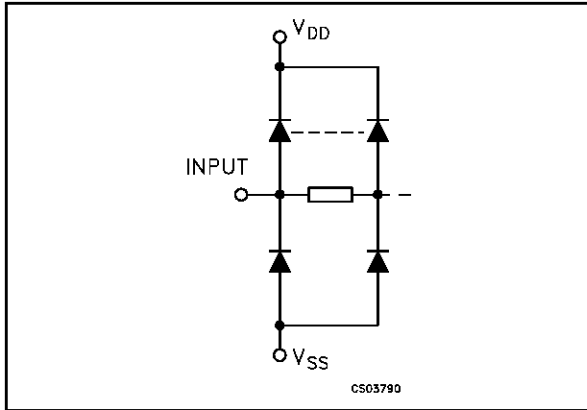
PACKAGE	TUBE	T & R
DIP	CC4038	

Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the negative going clock transition, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge. The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one bit position before the application of the first bit of the next word.

### PIN CONNECTION



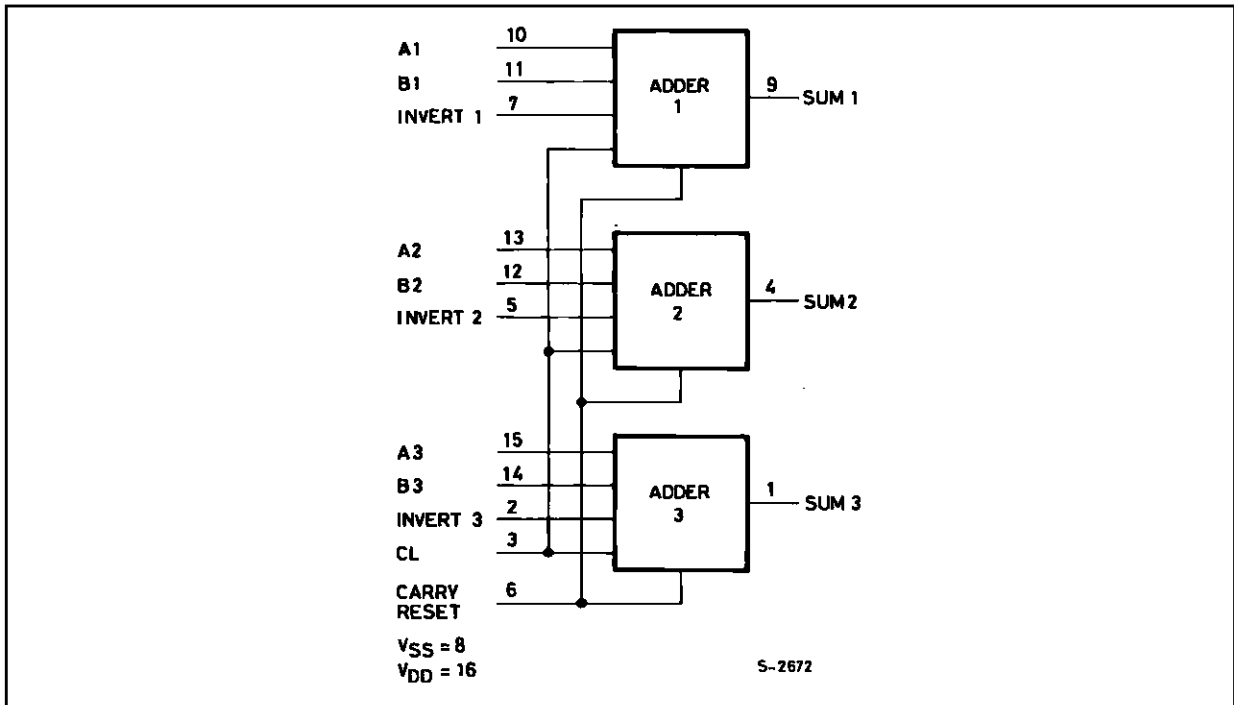
INPUT EQUIVALENT CIRCUIT



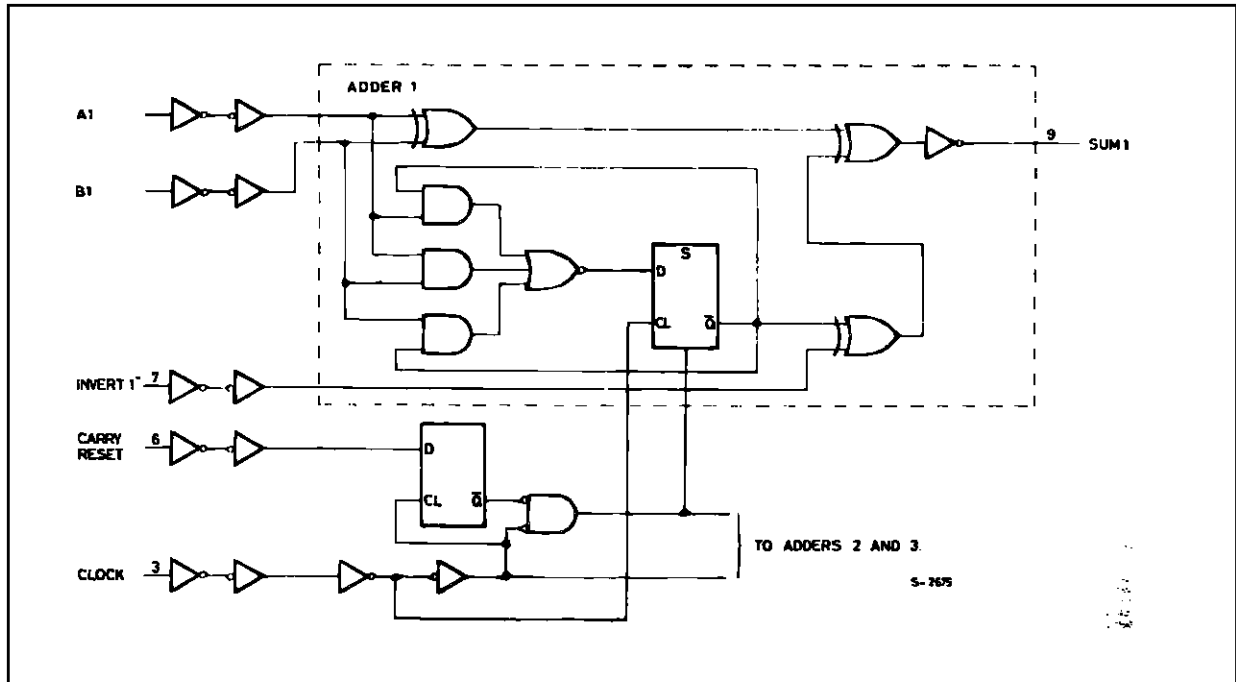
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
10, 13, 15	A1 to A3	Data Inputs
11, 12, 14	B1 to B3	Data Inputs
7, 5, 2	INVERT1 to INVERT3	Invert Command Inputs
9, 4, 1	SUM1 to SUM3	Data Outputs
3	CLOCK	Clock Input
6	CARRY-RESET	Carry Reset Input
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

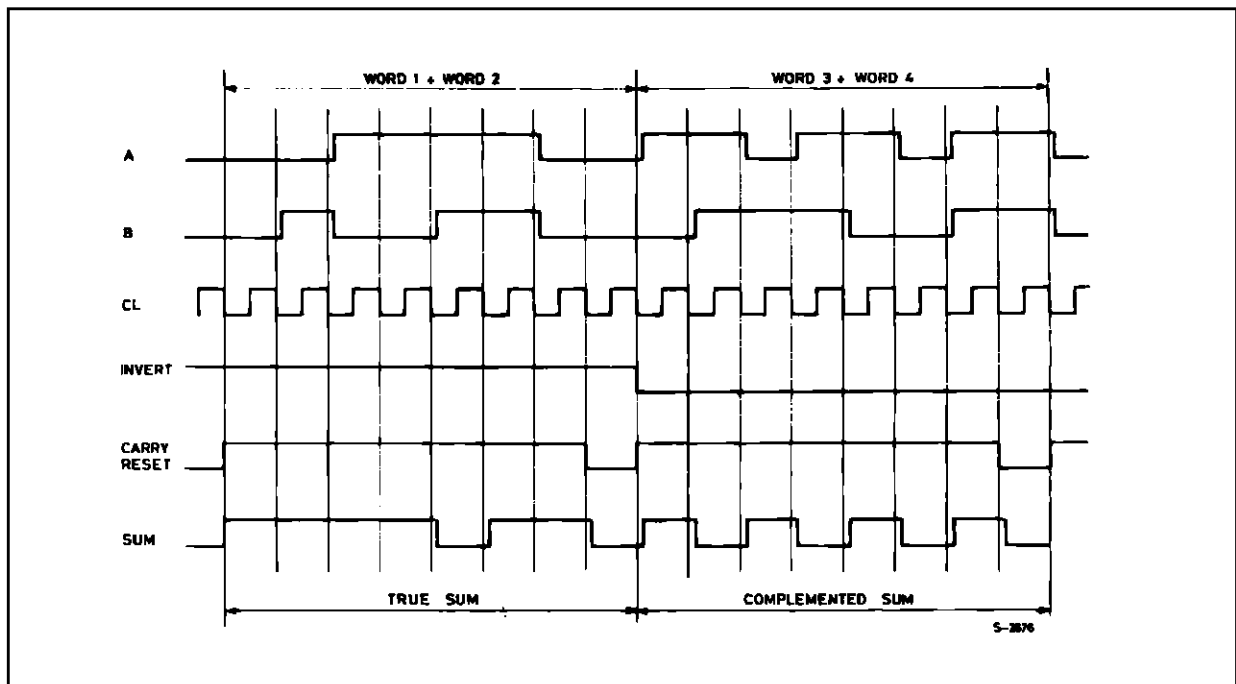
FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TIMING CHART



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +20	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 1.8	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

## DC SPECIFICATIONS

Symbol	Parameter	Test Conditions				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.04	5		150		150	$\mu$ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/18			18		0.08	100		3000		3000	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/18.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		0.5/4.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			1.5/18.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5		5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6		5	-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4		5	0.44	1		0.36		0.36		mA
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	any input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		any input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

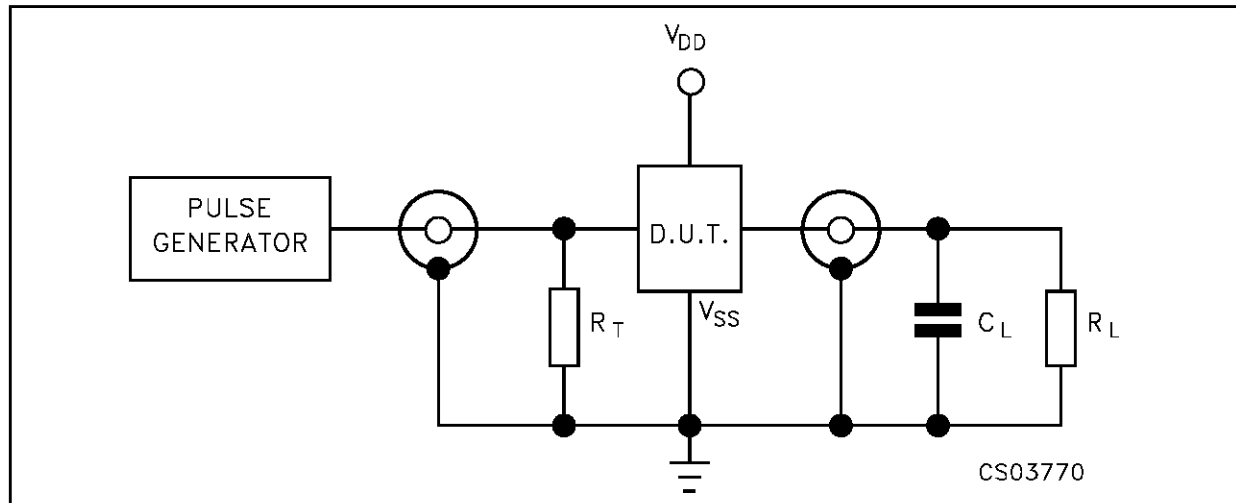
**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}C$ ,  $C_L = 50pF$ ,  $R_L = 200K\Omega$ ,  $t_r = t_f = 20 ns$ )

Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PHL}$ $t_{PLH}$	Propagation Delay Time (A, B or Inverter Inputs to Sum Outputs)	5			260	520	ns
		10			120	240	
		15			90	180	
$t_{PHL}$ $t_{PLH}$	Propagation Delay Time (Clock Inputs to Sum Outputs)	5			325	650	ns
		10			175	350	
		15			150	300	
$t_{THL}$ $t_{TLH}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$t_{hold}$	Data Input Hold Time (clock edge to A, B, or reset inputs)	5			120	200	ns
		10			50	80	
		15			40	60	
$f_{MAX}$	Maximum Clock Input Frequency	5		2.5	4.5		MHz
		10		5	10		
		15		7.5	15		
$t_r$ , $t_f$ (1)	Clock Input Rise or Fall Time	5				500	$\mu s$
		10				500	
		15				500	

(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.

(1) If more than one unit is cascaded  $t_r$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving state for the estimated capacitive load.

**TEST CIRCUIT**



$C_L = 50pF$  or equivalent (includes jig and probe capacitance)

$R_L = 200K\Omega$

$R_T = Z_{OUT}$  of pulse generator (typically 50 $\Omega$ )