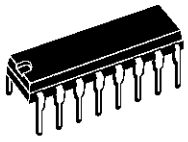
QUAD CLOCKED D LATCH

- CLOCK POLARITY CONTROL
- Q AND $\overline{Q}$ OUTPUTS
- COMMON CLOCK
- LOW POWER TTL COMPATIBLE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

ORDER CODES

PACKAGE	TUBE	T & R
DIP	CC4042	

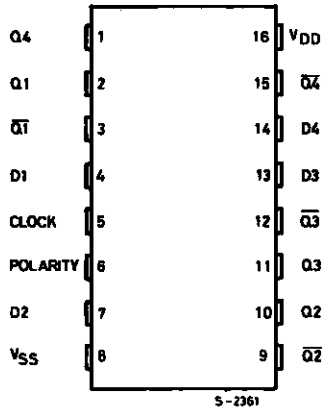
DESCRIPTION

The CC4042 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.

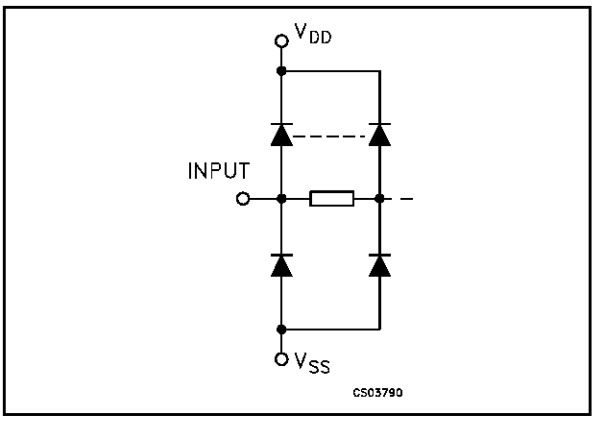
The CC4042 types contains four latch circuit, each strobes by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n and p channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

PIN CONNECTION



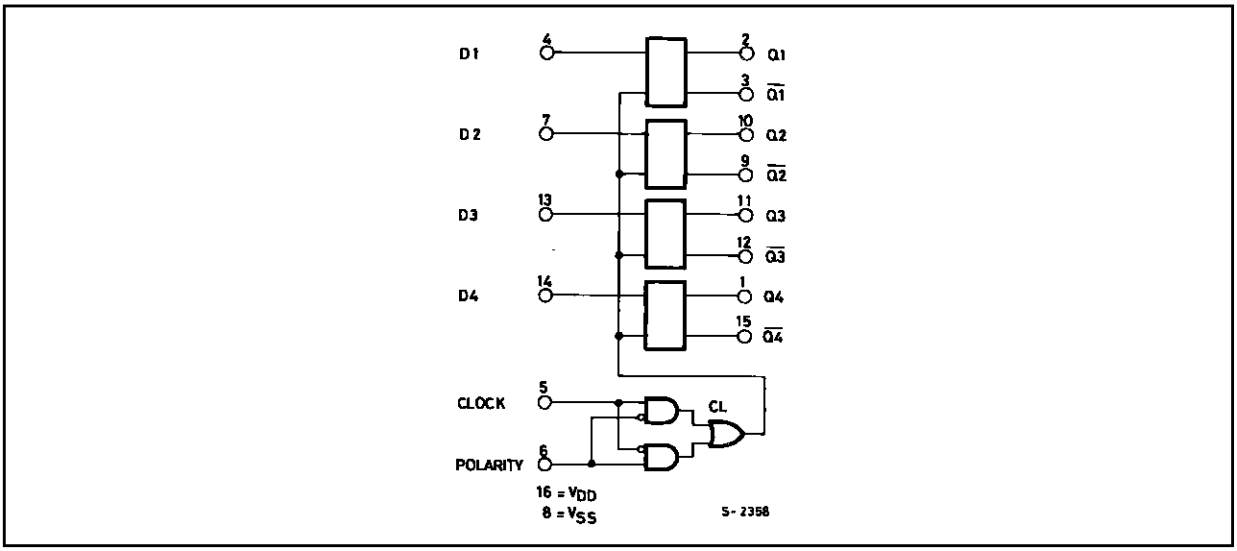
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
4, 7, 13, 14	D1 to D4	Data Inputs
2, 10, 11, 1	Q1 to Q4	Q outputs
3, 9, 12, 15	$\overline{Q1}$ to $\overline{Q4}$	$\overline{Q}$ outputs
5	CLOCK	Clock Input
6	POLARITY	Polarity inputs
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

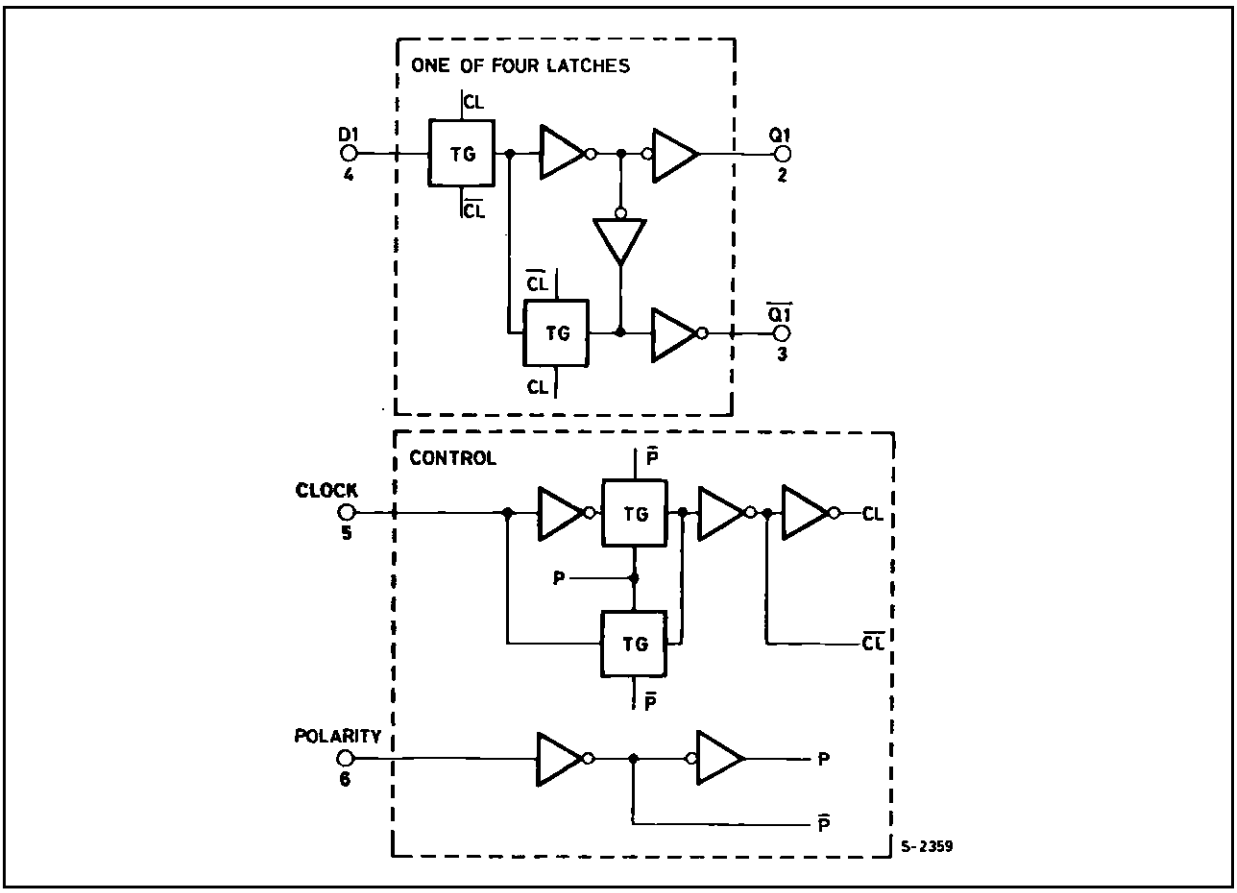
FUNCTIONAL DIAGRAM



TRUTH TABLE

CLOCK	POLARITY	Q
L	0	D
⌐	0	LATCH
H	1	D
¬	1	LATCH

LOGIC BLOCK DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 1 8	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.02	1		30		30	μA
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/18			18		0.04	20		600		600	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA IN to Q)	5			110	220	ns
		10			55	110	
		15			40	80	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA IN to $\overline{Q}$)	5			150	300	ns
		10			75	150	
		15			50	100	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK to Q)	5			225	450	ns
		10			100	200	
		15			80	160	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK to $\overline{Q}$)	5			250	500	ns
		10			115	230	
		15			90	180	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Clock Pulse Width	5		200	100		ns
		10		100	50		
		15		60	30		
t_{setup}	Setup Time	5		50	0		ns
		10		30	0		
		15		25	0		
t_{hold}	Hold Time	5			120	60	ns
		10			60	30	
		15			50	25	
t_r , t_f	Input Pulse Rise and Fall Time	5		Not Rise or Fall Time Sensitive			µs
		10					
		15					

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.