CC4504

Hex Level Shifter for TTL to CMOS or CMOS to CMOS

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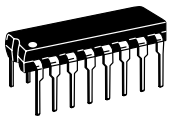
The MC14504B is a hex non–inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range



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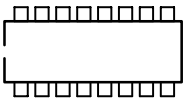


MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

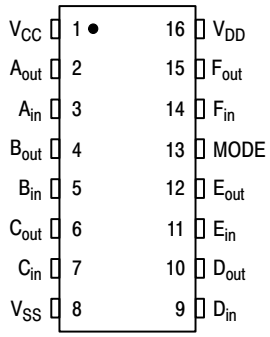
Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	–0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

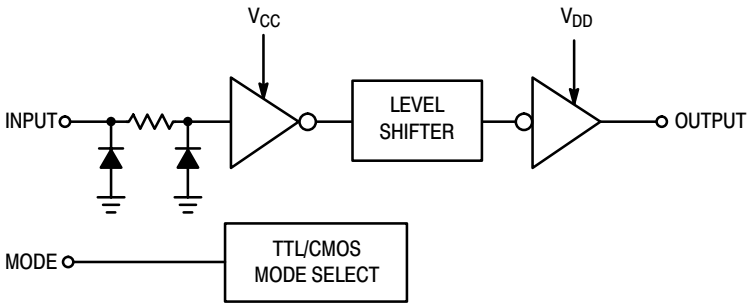
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	—	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = 0 V		—	10	—	0.05	—	0	0.05	—	0.05	
		—	1 5	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	—	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = V_{CC}		—	10	9.95	—	9.95	10	—	9.95	—	
		—	15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL–CMOS		5.0	10	—	0.8	—	1.3	0.8	—	0.8	
(V_{OL} = 1.5 Vdc) TTL–CMOS		5.0	15	—	0.8	—	1.3	0.8	—	0.8	
(V_{OL} = 1.0 Vdc) CMOS–CMOS		5.0	10	—	1.5	—	2.25	1.5	—	1.4	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		5.0	15	—	1.5	—	2.25	1.5	—	1.5	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		10	15	—	3.0	—	4.5	3.0	—	2.9	
Input Voltage “1” Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL–CMOS		5.0	10	2.0	—	2.0	1.5	—	2.0	—	
(V_{OH} = 13.5 Vdc) TTL–CMOS		5.0	15	2.0	—	2.0	1.5	—	2.0	—	
(V_{OH} = 9.0 Vdc) CMOS–CMOS		5.0	10	3.6	—	3.5	2.75	—	3.5	—	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		5.0	15	3.6	—	3.5	2.75	—	3.5	—	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		10	15	7.1	—	7.0	5.5	—	7.0	—	
Output Drive Current	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		—	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		—	5.0	–0.64	—	–0.51	– 0.88	—	–0.36	—	
(V_{OH} = 9.5 Vdc)		—	10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		—	15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	—	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		—	10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		—	15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	—	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD} or	—	5.0	—	0.05	—	0.0005	0.05	—	1.5	µAdc
(Per Package)	I_{CC}	—	10	—	0.10	—	0.0010	0.10	—	3.0	
CMOS–CMOS Mode		—	15	—	0.20	—	0.0015	0.20	—	6.0	
Quiescent Current	I_{DD}	5.0	5.0	—	0.5	—	0.0005	0.5	—	3.8	µAdc
(Per Package)		5.0	10	—	1.0	—	0.0010	1.0	—	7.5	
TTL–CMOS Mode		5.0	15	—	2.0	—	0.0015	2.0	—	15	
Quiescent Current	I_{CC}	5.0	5.0	—	5.0	—	2.5	5.0	—	6.0	mAdc
(Per Package)		5.0	10	—	5.0	—	2.5	5.0	—	6.0	
TTL–CMOS Mode		5.0	15	—	5.0	—	2.5	5.0	—	6.0	

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits			Unit
					Min	Typ (5.)	Max	
Propagation Delay, High to Low	t_{PHL}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15	— —	140 140	280 280	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15	— — —	120 120 70	240 240 140	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10	— — —	185 185 175	370 370 350	
Propagation Delay, Low to High	t_{PLH}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15	— —	170 160	340 320	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15	— — —	170 170 100	340 340 200	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10	— — —	275 275 145	550 550 290	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	— — —	5.0 10 15	— — —	100 50 40	200 100 80	ns

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