

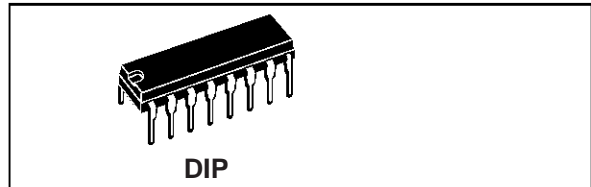


PRESETTABLE UP/DOWN COUNTERS

- MEDIUM SPEED OPERATION $f_{CL} = 8\text{MHz}$ TYP. AT 10V
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- RESET AND PRESET CAPABILITY
- QUIESCENT CURRENT SPECIFIED TO 15V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 15V AND 25°C
- 100% TESTED FOR QUIESCENT CURRENT MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

DESCRIPTION

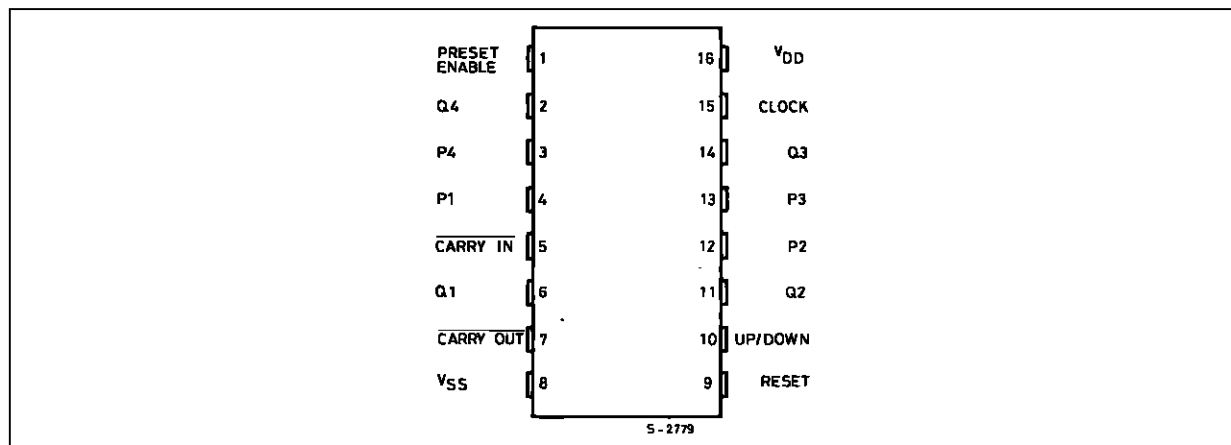
The CC4510 and CC4516 are monolithic integrated circuits available in 16-lead dual in-line plastic and plastic micro package. The HCF4510B Presettable BCD Up/Down Counter and the CC4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CC4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode,



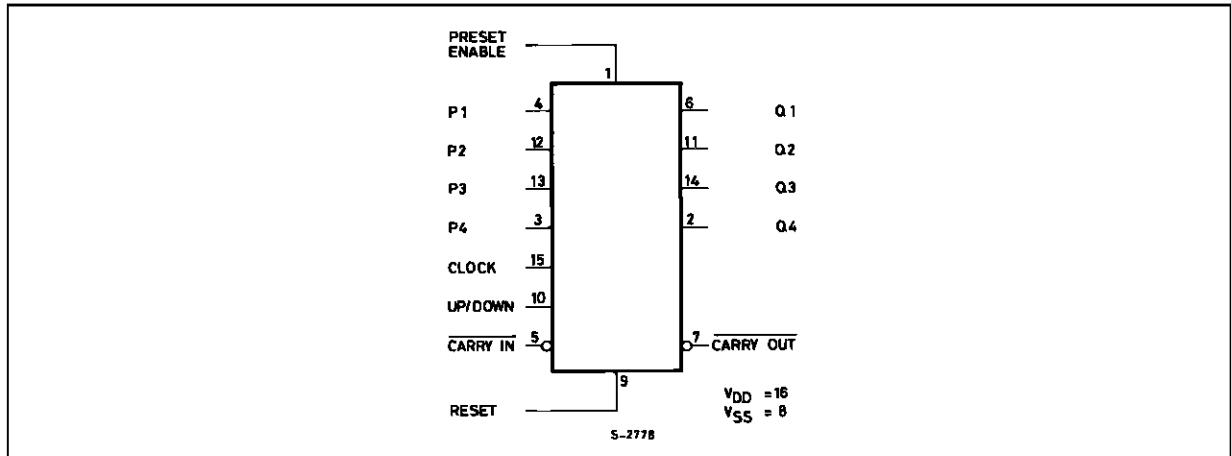
ORDER CODES		
PACKAGE	TUBE	T & R
DIP	CC45xx	

and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The CC4510 and CC4516 can be loaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

PIN CONNECTION



FUNCTIONAL DIAGRAM



TRUTH TABLE

CL	CI	U/D	PE	R	Action
X	1	X	0	0	No Count
	0	1	0	0	Count Up
	0	0	0	0	Count Down
X	X	X	1	0	Preset
X	X	X	X	1	Reset

X=Don't care

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{DD} *	Supply Voltage	-0.5 to +18	V
V _i	Input Voltage	-0.5 to V _{DD} + 0.5	V
I _i	DC Input Current (any one input)	± 10	mA
P _{tot}	Total Power Dissipation (per package)	200	mW
	Dissipation per Output Transistor for Top = Full Package Temperature Range	100	mW
T _{op}	Operating Temperature	-40 to +85	°C
T _{stg}	Storage Temperature	-65 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

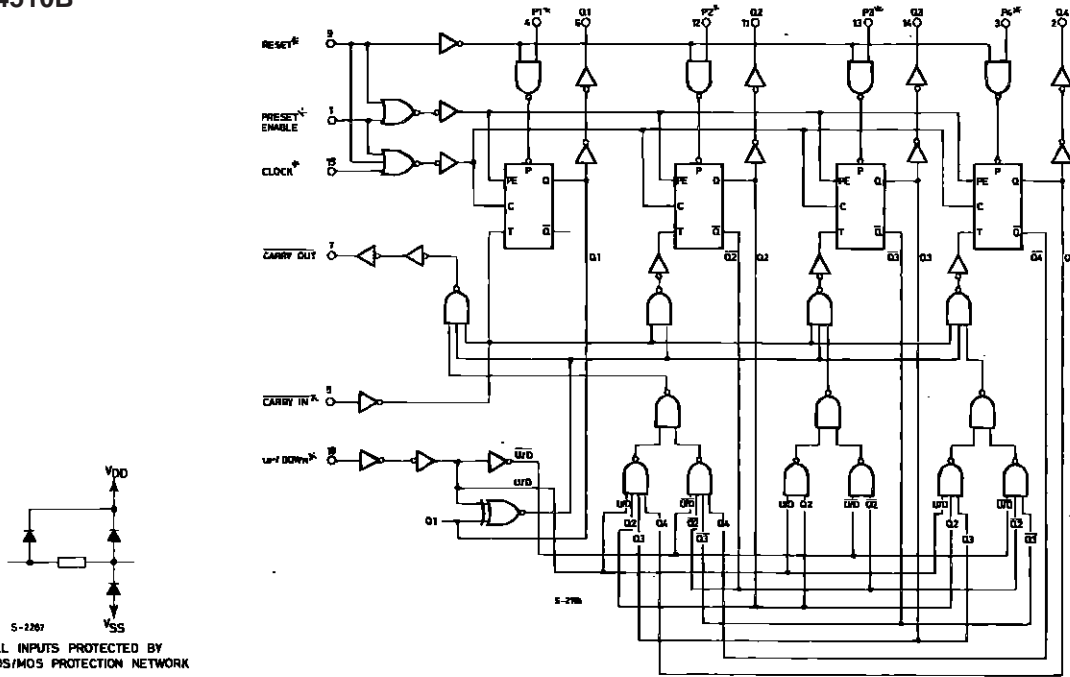
* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

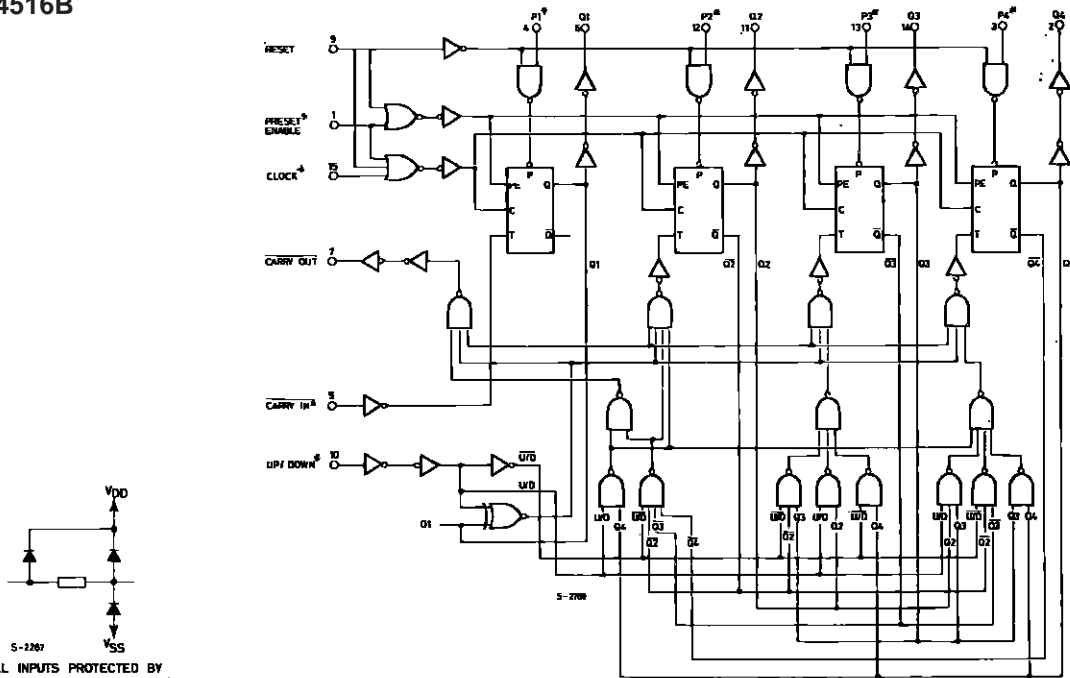
Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage	3 to 15	V
V _I	Input Voltage	0 to V _{DD}	V
T _{op}	Operating Temperature	-40 to +85	°C

LOGIC DIAGRAMS

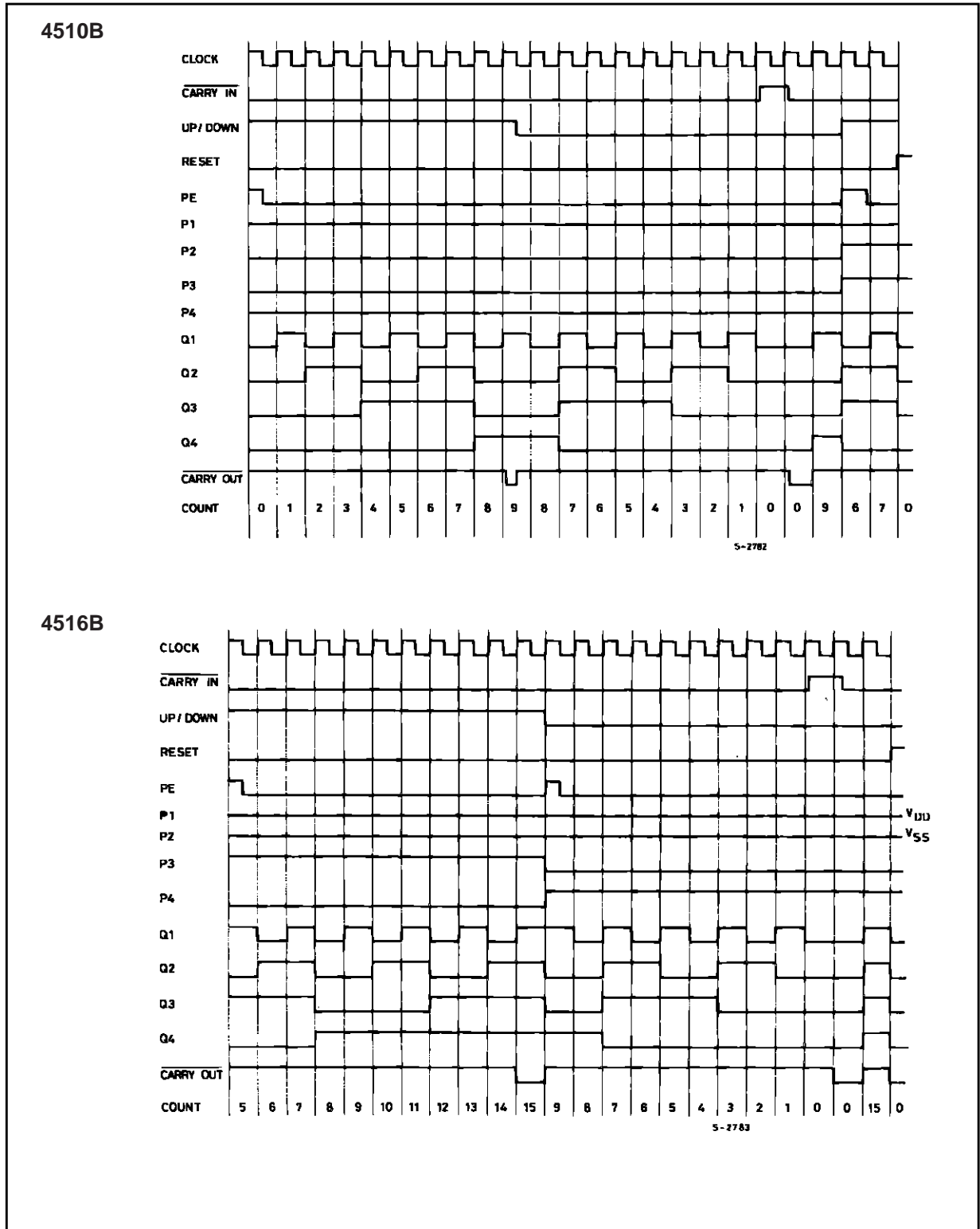
4510B



4516B



TIMING DIAGRAMS



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter	Test Conditions				Value						Unit	
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	-40 °C		25 °C			85 °C		
						Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _L	Quiescent Current	0/5			5		20		0.02	20		150	μ A
		0/10			10		40		0.02	40		300	
		0/15			15		80		0.02	80		600	
V _{OH}	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V _{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V _{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V _{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I _{OH}	Output Drive Current	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		mA
		0/5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output Sink Current	0/5	0.4		5	0.52		0.44	1		0.36		mA
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input Leakage Current	0/15	Any Input		15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	μ A
C _I	Input Capacitance		Any Input						5	7.5			pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$, typical temperature coefficient for all V_{DD} values is $03\text{ }^{\circ}\text{C}$, all input rise and fall times = 20 ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q Output		5		200	400	ns
			10		100	200	
			15		75	150	
t_{PHL} t_{PLH}	Propagation Delay Time Preset or Reset to Q Output		5		210	420	ns
			10		105	210	
			15		80	160	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Carry Out		5		240	480	ns
			10		120	240	
			15		90	180	
t_{PHL} t_{PLH}	Propagation Delay Time Carry In to Carry Out		5		125	250	ns
			10		60	120	
			15		50	100	
t_{PHL} t_{PLH}	Propagation Delay Time Preset or Reset to Carry Out		5		320	640	ns
			10		160	320	
			15		125	250	
t_{THL} t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
f_{MAX}	Max Clock Frequency		5	2	4		MHz
			10	4	8		
			15	5.5	11		
t_w	Clock Pulse Width		5	150			ns
			10	75			
			15	60			
	Preset Enable or Reset Removal Time (1)		5	150			ns
			10	80			
			15	60			
t_r, t_f	Clock Rise and Fall Time (2)		5			15	μs
			10			5	
			15			5	
t_{setup}	Carry In Setup Time		5	130			ns
			10	60			
			15	45			
t_{setup}	Up Down Setup Time		5	360			ns
			10	160			
			15	110			
t_w	Preset Enable or Reset Pulse Width		5	220			ns
			10	100			
			15	75			

(1) Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

(2) If more than unit is cascaded in the parallel clocked application, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage of the estimated capacitive load.