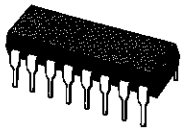
上海双岭电子有限公司

CC4527

BCD RATE MULTIPLEXER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO 9 INPUT AND 9 DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES "

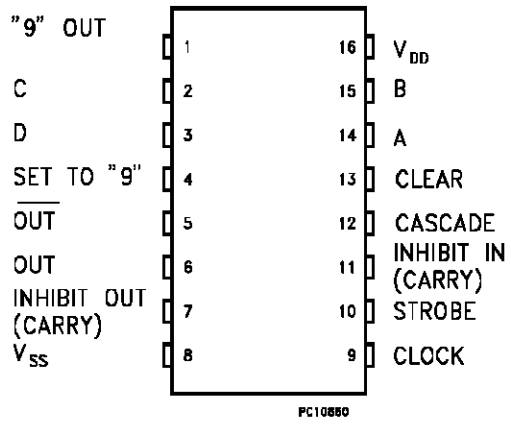


DESCRIPTION

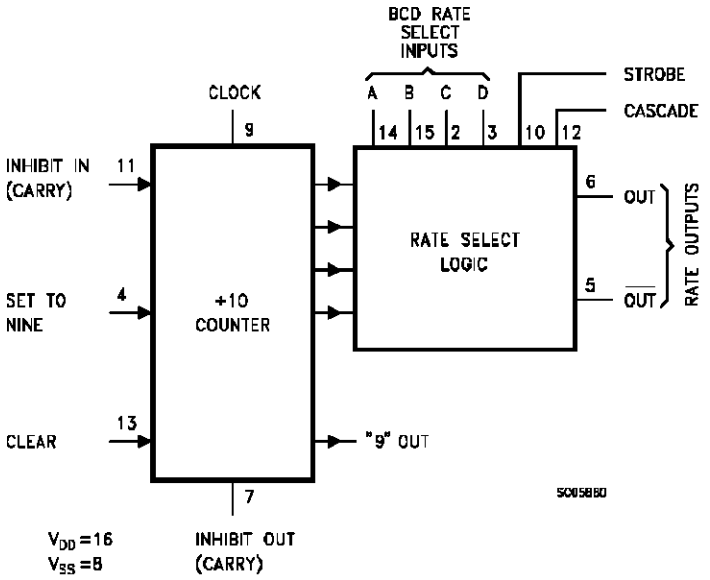
The **CC4527** (extended temperature range) and **CC4527** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in line plastic or ceramic package.

The **CC4527** is a low power 4 bit digital rate multiplier that provides an output pulse rate which is the clock input pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to preform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate naturel logarithms and trigonometric func-

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD} *	Supply Voltage:	-0.5 to +20	V
V_i	Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200 100	mW mW
T_{op}	Operating Temperature:	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

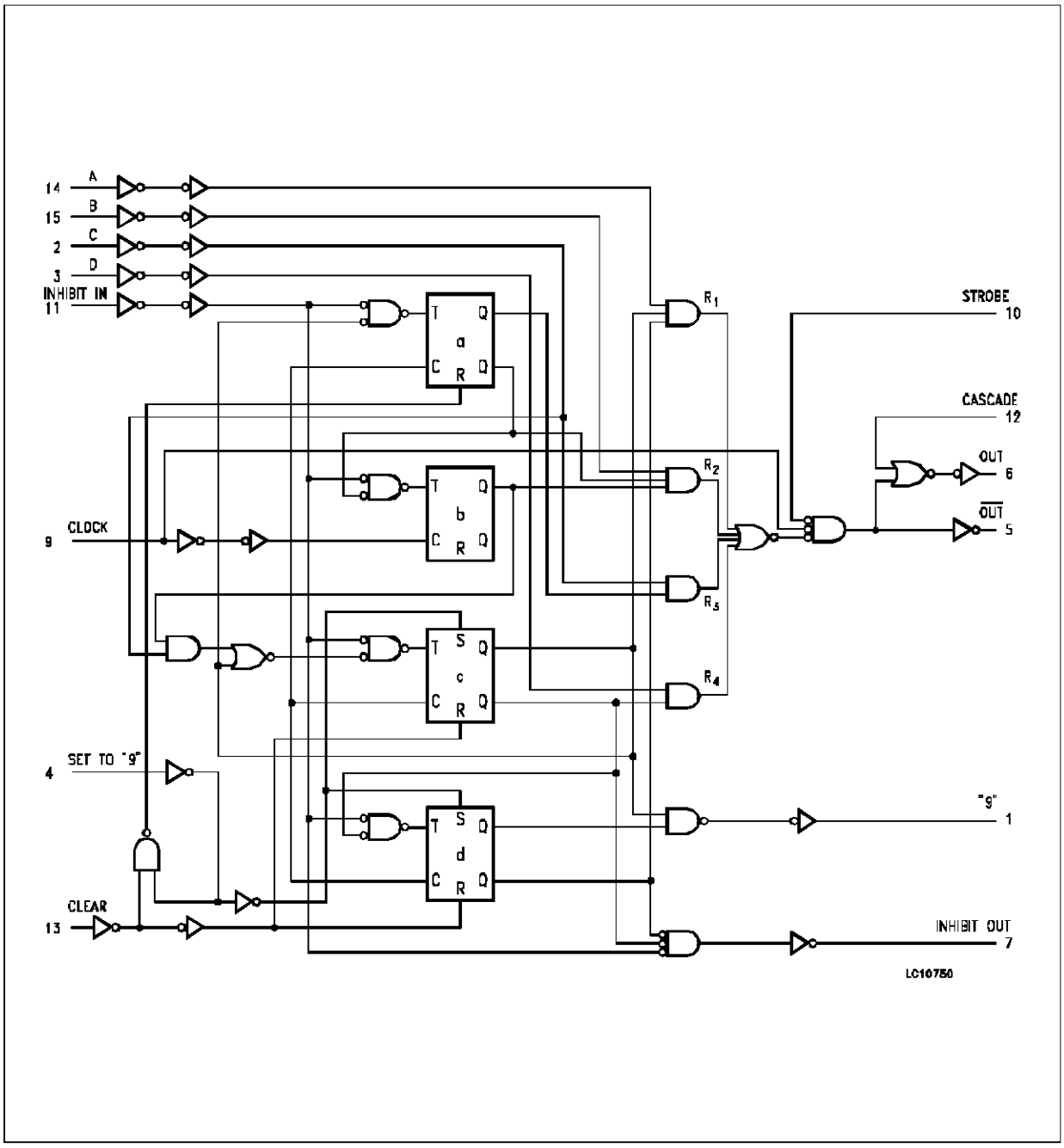
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage:	3 to 18	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature:	-55 to +125	°C

LOGIC DIAGRAM



TRUTH TABLE

Inputs										Outputs			
Number of Pulsed or Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = LOW; H = High)			
D	**C**	**B**	**A**	**CLK**	**INH IN**	**STR**	**CAS**	**CLR**	**SET**	**OUT**	**$\overline{\text{OUT}}$**	**INH OUT**	**"9" OUT**
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	■	■	H	■
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	●	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

● Output same as the first 16 lines of this truth table (depending on value of A, B, C, D)

■ Depends on internal state of counter.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditios				Value							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_{LOW} * Min.	T_{LOW} * Max.	25 °C Min.	25 °C Typ.	25 °C Max.	T_{HIGH} * Min.	T_{HIGH} * Max.	
I_L	Quiescent Current		0/5			5		5		0.04	5		150	µA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/18			18		100		0.08	100		3000	
V_{OH}	Output High Voltage		0/5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current		0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
I_{OL}	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current		0/18	Any Input		18		±0.1		$±10^{-5}$	±0.1		±1	µA
C_I	Input Capacitance			Any Input						5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 ^{o}C, C_L = 50 pF, R_L = 200 KΩ, typical temperature coefficent for all V_{DD} values is 03 %/^{o}C, all input rise and fall times= 20 ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to Output)		5		110	220	ns
			10		55	110	
			15		45	90	
t_{PLH} t_{PHL}	Propagation Delay Time Clock or Strobe to Output		5		150	300	ns
			10		75	150	
			15		60	120	
t_{PLH}	Propagation Delay Time Clock to Inhibit Output		5		320	640	ns
			10		145	290	
			15		100	200	
t_{PHL}	Propagation Delay Time Clock to Inhibit Output		5		250	500	ns
			10		100	200	
			15		75	150	
t_{PLH} t_{PHL}	Propagation Delay Time Clear to Output		5		380	760	ns
			10		175	550	
			15		130	260	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to ”9” or ”1” Q Output		5		300	600	ns
			10		125	250	
			15		90	180	
t_{PLH} t_{PHL}	Propagation Delay Time Cascade to Output		5		90	180	ns
			10		45	90	
			15		35	70	
t_{PLH} t_{PHL}	Propagation Delay Time Inhibit Input to Inhibit Output		5		130	260	ns
			10		60	120	
			15		45	90	
t_{PLH} t_{PHL}	Propagation Delay Time Set to Output		5		330	660	ns
			10		150	300	
			15		110	220	
t_{THL} t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
f_{CL}	Maximum Clock Frequency		5	1.2	2.4		MHz
			10	2.5	5		
			15	3.5	7		
t_W	Clock Pulse Width		5	330	165		ns
			10	170	85		
			15	100	50		
t_r, t_f	Clock Rise or Fall Time		5			15	µs
			10			15	
			15			15	
t_W	Set or Clear Pulse Width		5	160	80		ns
			10	90	45		
			15	60	30		
t_{setup}	Inhibit Input Setup Time		5	100	50		ns
			10	40	20		
			15	20	10		