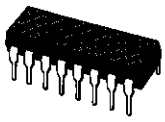
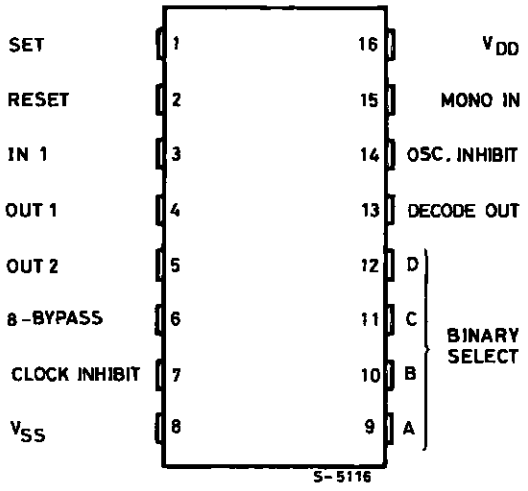
CC4536

PROGRAMMABLE TIMER

- 24 FLIP-FLOP STAGES - COUNTS FROM 2^0 TO 2^{24}
- LAST 16 STAGES SELECTABLE BY BCD SELECT CODE
- BYPASS INPUT ALLOWS BYPASSING FIRST 8 STAGES
- ON-CHIP RC OSCILLATOR PROVISION
- CLOCK INHIBIT INPUT
- SCHMITT-TRIGGER IN CLOCK LINE PERMITS OPERATION WITH VERY LONG RISE AND FALL TIMES
- ON-CHIP MONOSTABLE OUTPUT PROVISION
- TYPICAL f_{CL} = 3MHz AT V_{DD} = 10V
- TEST MODE ALLOWS FAST TEST SEQUENCE
- SET AND RESET INPUTS
- CAPABLE OF DRIVING TWO LOW POWER TTL LOADS, ONE LOWER-POWER SCHOTTKY LOAD, OR TWO HTL LOADS OVER THE RATED TEMPERATURE RANGE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



PIN CONNECTIONS

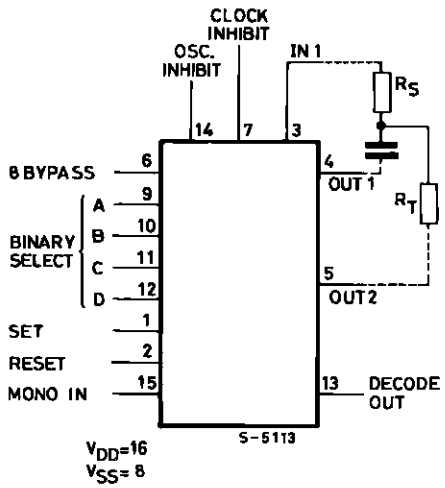


DESCRIPTION

The **CC4536** (extended temperature range) and **CC4536** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **CC4536** is a programmable timer consisting of 24 ripple-binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to 2^{24} or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components.

Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities. A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10KΩ or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to V_{DD} and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width. A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

FUNCTIONAL DIAGRAM

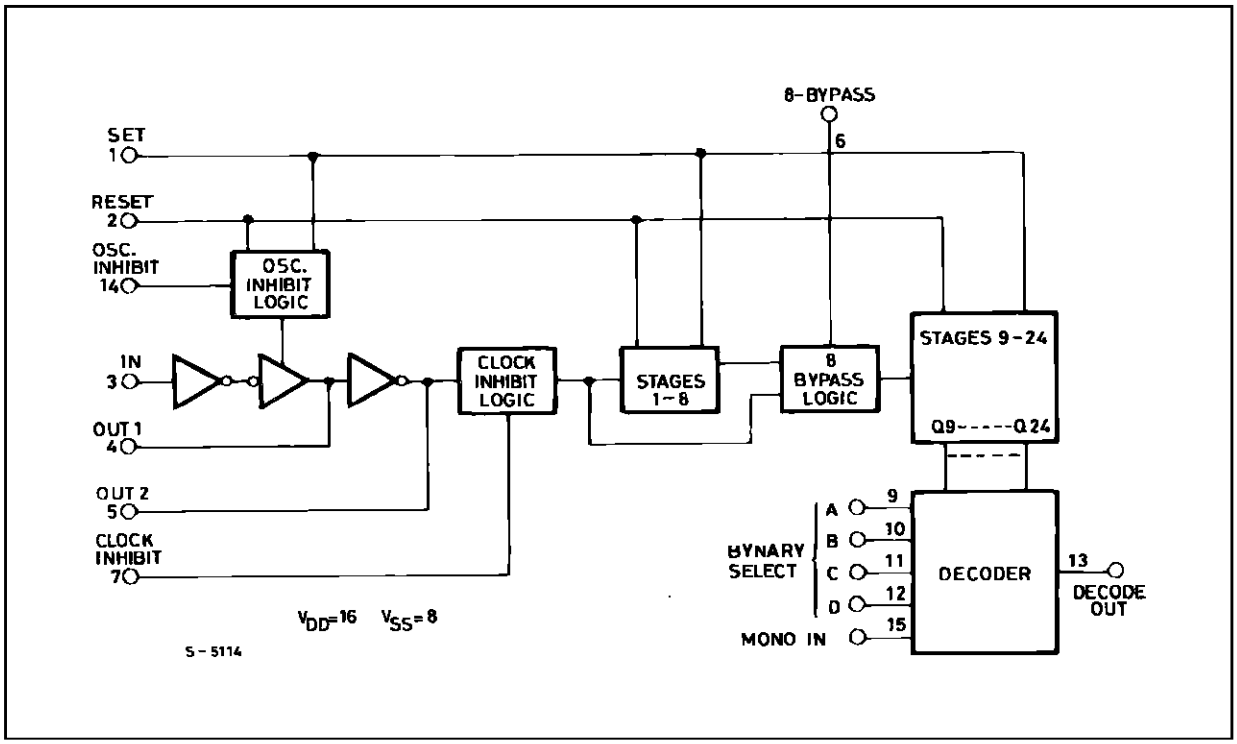


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage :	– 0.5 to + 20	V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature :	– 55 to + 125	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to V_{SS} (GND).

BLOCK DIAGRAM



TRUTH TABLE

In1	Set	Reset	Clock Inh	Osc Inh	Out1	Out2	Decode Out
⎍	0	0	0	0	⎍	⎏	No Change
⎏	0	0	0	0	⎏	⎍	Advance to Next State
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⎍	⎏	⎍	Advance to Next State

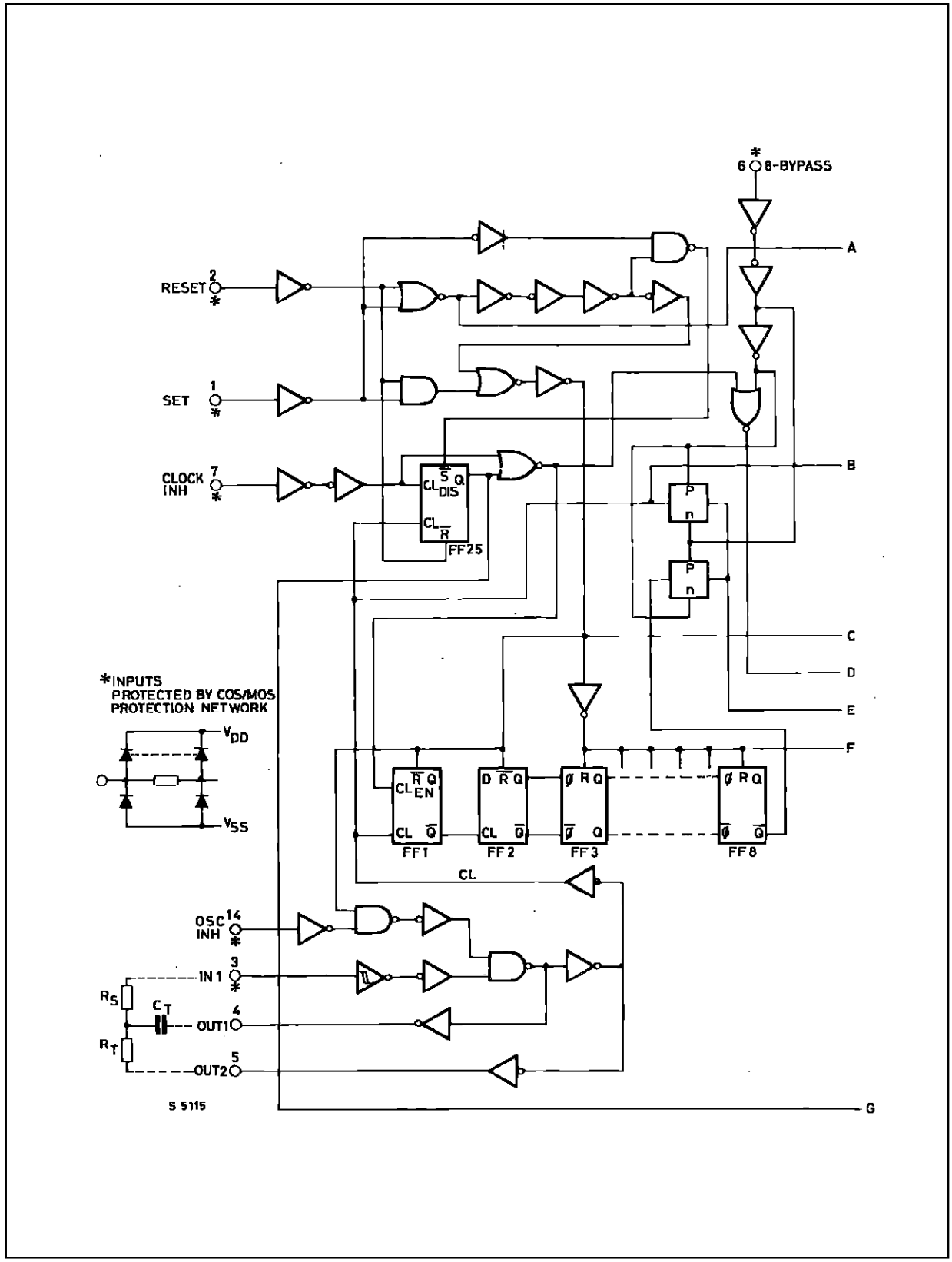
0 = Low Level

DECODE OUT SELECTION TABLE

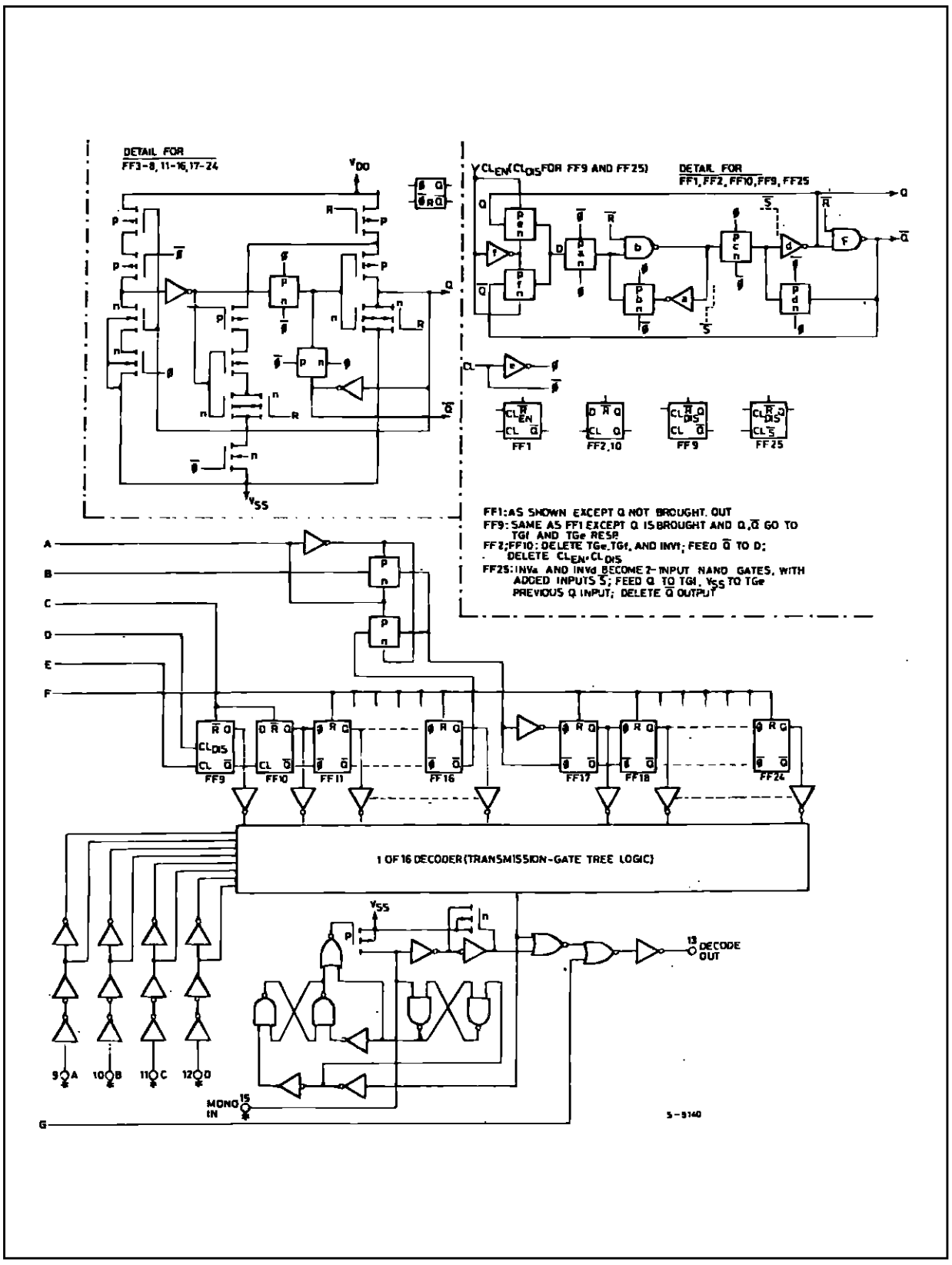
D	C	B	A	Number or Stages In Divider Chain	
				8-BYPASS = 0	8-BYPASS = 1
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

0 = Low Level

LOGIC DIAGRAMS (continued on next page)



LOGIC DIAGRAMS (continued)



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Current	Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/18			18		100		0.08	100		3000	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	Types	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
I_{OL}	Output Sink Current	Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_I	Input Capacitance			Any Input						5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 ^{o}C, C_L = 50 pF, R_L = 200 KΩ, typical temperature coefficent for all V_{DD} values is 03 %/^{o}C, all input rise and fall times= 20 ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to Q1, 8-bypass High		5		1	2	µs
			10		0.5	1	
			15		0.35	0.7	
	Clock to Q1, 8-bypass Low		5		2.5	5	µs
			10		0.8	1.6	
			15		0.6	1.2	
	Clock to Q16		5		4	8	µs
			10		1.5	3	
			15		1	2	
	Q_n to Q_{n+1}		5		150	300	ns
			10		75	150	
			15		50	100	
t_{PLH}	Propagation Delay Time		5		300	600	ns
			10		125	250	
			15		80	160	
t_{PHL}	Reset to Qn		5		3	6	µs
			10		1	2	
			15		0.75	1.5	
t_{TLH} t_{THL}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Pulse Width Clock		5		200	400	ns
			10		75	150	
			15		50	100	
	Set		5		200	400	ns
			10		100	200	
			15		60	120	
	Reset		5		3	6	µs
			10		1	2	
			15		0.75	1.5	
	Recovery Time Set		5		2.5	5	µs
			10		1	2	
			15		0.6	1.6	
	Reset		5		3.5	7	µs
			10		1.5	3	
			15		1	2	
t_r, t_f	Clock Input Rise or Fall Time		5	Unlimted			µs
			10				
			15				
f_{CL}	Maximum Clock Input Frequency			0.5	1		MHz
			10	1.5	3		
			15	2.5	5		